UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,085	03/29/2001	Jingsheng Jason Cong	004120.P005	6979

7590 01/24/2005

Michael J. Mallie
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/823,085	CONG ET AL.	
	Examin r	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communicati n appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,8,10 and 21* is/are allowed.

6)☒ Claim(s) *1-3,7,9,11-14,20 and 22-33* is/are rejected.

7)☒ Claim(s) *4,5 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

DETAILED ACTION

1. This communication is in response to the Applicants' amendment dated October 1, 2004. Claims 4, 6, 7, 8, 10,15, 17, 18, 19, 21, 26, 28, 29, 30 and 32 were amended. Claims 1-33 of the application are pending in the application. This office action is made non-final.

Drawings

2. The formal drawings submitted on October 1, 2004 are accepted.

Claim Objections

3. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

4. Claims 17-1921 are objected to because of the following informalities:

Amended Claim 17, Lines 6-8, "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and instructions to determine noise width" appears to be incorrect

and it appears it should be "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and to determine noise width".

Amended Claim 18, Lines 6-8, "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and instructions to determine noise width" appears to be incorrect and it appears it should be "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and to determine noise width".

Amended Claim 19, Lines 6-8, "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and instructions to determine noise width" appears to be incorrect and it appears it should be "model the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor and to determine noise width".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make

and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 23-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6.1 Claim 23 states, "An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design".

However, the specification does not describe anywhere the means used for locating a victim net and an aggressor within the integrated circuit design, means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc. If the

applicants believe that the specification describes the means used by the apparatus, they are directed to indicate the page and paragraphs where the means are described and the figures which show the components of the means.

6.2 Claim 24 states, "The apparatus defined in Claim 23 wherein the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location".

However, the specification does not describe anywhere the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits and the means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.3 Claim 25 states, "The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises means for determining noise width".

However, the specification does not describe anywhere the means for modeling the victim net and the means for determining noise width, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.4 Claim 28 states, "An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design; means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for determining noise width, wherein the noise width is determined corresponding to:

$$t_r + t_v \ln[(1- e^{-2t_r/t_v})/ (1- e^{-t_r/t_v})]$$

where t_r comprises transition time and t_v comprises a distributed Elemore delays of the victim net; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design".

However, the specification does not describe anywhere the means for locating a victim net and an aggressor within the integrated circuit design; means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor; means for determining noise width; and means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.5 Claim 29 states, "An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for determining noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design".

However, the specification does not describe anywhere the means for locating a victim net and an aggressor within the integrated circuit design; means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor; means for determining noise width; and means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.6 Claim 30 states, "An apparatus for identifying potential noise failures in an integrated circuit design comprising:

means for locating a victim net and an aggressor within the integrated circuit design;

means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor and means for determining noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location; and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design".

However, the specification does not describe anywhere the means for locating a victim net and an aggressor within the integrated circuit design; means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor; means for determining noise width; and means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.7 Claim 31 states, "The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises means for determining the peak noise amplitude".

However, the specification does not describe anywhere the means for modeling the victim net and the means for determining the peak noise amplitude, in terms of the hardware

elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

6.8 Claim 33 states, "The apparatus defined in Claim 23 wherein the means for modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path".

However, the specification does not describe anywhere the means for modeling the victim net, in terms of the hardware elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc.

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1, 2, 9, 12, 13, 20, 23, 24 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Rao** ("Delay analysis of the distributed RC line", IEEE, 1995).

9.1 **Aingaran et al.** teaches two pole coupling noise analysis model for submicron integrated circuit design verification. Specifically, as per claim 23, **Aingaran et al.** teaches an apparatus for identifying potential noise failures in an integrated circuit design (Abstract, L1-18; Fig 6; CL3, L48-53); comprising:

means for locating a victim net and an aggressor within the integrated circuit design (Abstract, L5-9); and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design (Abstract, L12-18).

Aingaran et al. teaches means for modeling the victim net using single π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor (CL5, L14-22). **Aingaran et al.** does not expressly teach means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor. **Rao** teaches means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor (Page 5, CL1, Para 1, L7-14 and L30-35; Page 5, CL2, Para 2, L1-3 and L12-16; page 5, table 2; Page 6, Fig 2(c)), as higher order lumped approximations of distributed resistance and capacitance provide accurate predictions of 10% and 90% threshold crossing times; and the first order network underestimates the 10% crossing time by as much as 60%, while the second order network underestimates the 10% crossing time less than 22% (Page 1, CL1, Para 1, L12-15; Page 5, CL2, Para 2, L1-3 and L12-16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Rao** that included means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor. The artisan would have been motivated because higher order lumped approximations of distributed resistance and capacitance would provide accurate predictions of 10% and 90% threshold crossing times; and the first order network would underestimate the 10% crossing time by as much as 60%, while the second order network would underestimate the 10% crossing time less than 22%.

9.2 As per claim 24, **Aingaran et al.**. and **Rao** teach the apparatus of claim 23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location. **Rao** teaches that the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location (Page 5, CL1, Para 1, L7-14 and L30-35; Page 5, CL2, Para 2, L1-3 and L12-16; page 5, table 2; Page 6, Fig 2(c)), as higher order lumped approximations of distributed resistance and capacitance provide accurate predictions of 10% and 90% threshold crossing times; and the first order network underestimates the 10% crossing time by as much as 60%, while the second order network underestimates the 10% crossing time less than 22% (Page 1, CL1, Para 1, L12-15; Page 5, CL2, Para 2, L1-3 and L12-16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Rao** that included the means for modeling the victim net using two π-type resistor-capacitor (RC) circuits comprising means for modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location. The artisan would have been motivated because higher order lumped approximations of distributed resistance and capacitance would provide accurate predictions of 10% and 90% threshold crossing times; and the first order network would underestimate the 10% crossing time by as much as 60%, while the second order network would underestimate the 10% crossing time less than 22%..

9.3 As per claim 31, **Aingaran et al.** and **Rao** teach the apparatus of claim 23. **Aingaran et al.** also teaches that the means for modeling the victim net comprises means for determining the peak noise amplitude (CL6, L50-56; CL10, L27-37).

9.4 As per Claims 1, 2, 9, 12, 13 and 20, these are rejected based on the same reasoning as Claims 23, 24 and 31, supra. Claims 1, 2, 9, 12, 13 and 20 are method and article of manufacture comprising one or more recordable medium claims reciting the same limitations as Claims 23, 24 and 31, as taught throughout by **Aingaran et al.** and **Rao.**

10. Claims 3, 14 and 25 are rejected under 35 U.S.C. 103(a) under 35 U.S.C. 103(a) as being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Rao** ("Delay analysis of the distributed RC line", IEEE, 1995), and further in view of **Huang** (U.S. Patent 5,568,395).

10.1 As per claim 25, **Aingaran et al.** and **Rao** teach the apparatus of claim 23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net comprises means for determining noise width. **Huang** teaches that the means for modeling the victim net comprises means for determining noise width (Cl14, L25-46; CL20, L66 to CL21, L1), as false logic error occurs when false logic noise height and noise width exceed the thresholds specified for the particular technology (CL14, L34-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Huang** that included the means for modeling the victim net comprising means for determining noise width. The artisan would have been motivated because false logic error

occurs when false logic noise height and noise width exceed the thresholds specified for the particular technology.

10.2 As per Claims 3 and 14, these are rejected based on the same reasoning as Claim 25, supra. Claims 3 and 14 are method and article of manufacture comprising one or more recordable medium claims reciting the same limitations as Claim 25, as taught throughout by **Aingaran et al., Rao** and **Huang.**

11. Claims 7, 18 and 29 are rejected under 35 U.S.C. 103(a) under 35 U.S.C. 103(a) as being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of in view of **Rao** ("Delay analysis of the distributed RC line", IEEE, 1995), and further in view of **Heijningen et al.** (U.S. Patent application 2002/0022951) and **Alpert et al.** (U.S. Patent 6,117,182).

11.1 As per claim 29, **Aingaran et al.** teaches an apparatus for identifying potential noise failures in an integrated circuit design (Abstract, L1-18; Fig 6; CL3, L48-53); comprising:

means for locating a victim net and an aggressor within the integrated circuit design (Abstract, L5-9); and

means for indicating that the integrated circuit design requires modification if modeling the victim net indicates that a potential noise failure may occur in the integrated circuit design (Abstract, L12-18).

Aingaran et al. teaches means for modeling the victim net using single π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor (CL5, L14-22). **Aingaran et al.** does not expressly teach means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor. **Rao** teaches means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor (Page 5, CL1, Para 1, L7-14 and L30-35; Page 5, CL2, Para 2, L1-3 and L12-16; page 5, table 2; Page 6, Fig 2(c)), as higher order lumped approximations of distributed resistance and capacitance provide accurate predictions of 10% and 90% threshold crossing times; and the first order network underestimates the 10% crossing time by as much as 60%, while the second order network underestimates the 10% crossing time less than 22% (Page 1, CL1, Para 1, L12-15; Page 5, CL2, Para 2, L1-3 and L12-16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Rao** that included means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor. The artisan would have been motivated because higher order lumped approximations of distributed resistance and capacitance would provide accurate predictions of 10% and 90% threshold crossing times; and the first order network would underestimate the 10% crossing time by as much as 60%, while the second order network would underestimate the 10% crossing time less than 22%.

Aingaran et al. does not expressly teach that the noise width is based on transition time. **Heijningen et al.** teaches that the noise width is based on transition time (Page 3, Para 0037), as

the input transition time determines the maximum amplitude and pulse width of the noise contributions (Page 3, Para 003). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Heijningen et al.** that included the noise width being based on transition time. The artisan would have been motivated because the input transition time would determine the maximum amplitude and pulse width of the noise contributions.

Aingaran et al. does not expressly teach that the noise width is based on distributed Elmore delay of the victim net. **Alpert et al.** teaches that the noise width is based on distributed Elmore delay of the victim net (Abstract L2-9; CL2, L55-56; CL3, L1-2), as Elmore delay model can be used for calculating the circuit noise and determining if the noise exceeds the acceptable limit so buffer insertion can be made (Abstract L2-9; CL2, L55-56). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Alpert et al.** that included the noise width being based on distributed Elmore delay of the victim net. The artisan would have been motivated because Elmore delay model could be used for calculating the circuit noise and determining if the noise exceeded the acceptable limit so buffer insertion could be made.

11.2 As per Claims 7 and 18, these are rejected based on the same reasoning as Claim 29, supra. Claims 7 and 18 are method and article of manufacture comprising one or more recordable medium claims reciting the same limitations as Claim 259 as taught throughout by **Aingaran et al., Rao, Heijningen et al.** and **Alpert et al.**

12. Claims 11, 22 and 33 are rejected under 35 U.S.C. 103(a) under 35 U.S.C. 103(a) as being unpatentable over **Aingaran et al.** (U.S. Patent 6,536,022) in view of **Rao** ("Delay analysis of the distributed RC line", IEEE, 1995), and further in view of and **Alpert et al.** (U.S. Patent 6,117,182).

12.1 As per claim 33, **Aingaran et al** and **Rao** teach the apparatus of claim 23. **Aingaran et al.** does not expressly teach that the means for modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path. **Alpert et al.** teaches that the means for modeling the victim net comprises computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path (CL6, L52-60; CL10, L12-20), because the net consists of a source and a sink; the aggressor net transmits aggressor pulse into the victim net due to coupling capacitance which is proportional to the distance the aggressor net and the victim net run parallel to each other (CL6, L52-60). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Aingaran et al.** with the apparatus of **Alpert et al.** that included the means for modeling the victim net comprising computing crosstalk noise at a sink with a lumped capacitance at each branch incorporated on a path from a source to the sink, with lumped capacitances being added in a weighted manner based on their locations on the path. The artisan would have been motivated because the net would consist of a source and a sink; the aggressor net would transmit aggressor pulse into the victim net due to

coupling capacitance which would be proportional to the distance the aggressor net and the victim net run parallel to each other.

12.2 As per Claims 11 and 22, these are rejected based on the same reasoning as Claim 33, supra. Claims 11 and 22 are method and article of manufacture comprising one or more recordable medium claims reciting the same limitations as Claim 33, as taught throughout by **Aingaran et al., Rao** and **Alpert et al.**

Allowable Subject Matter

13. Claims 4, 5, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if claim 4 is rewritten to depend on claim 6 and claim 15 is rewritten to depend on claim 17.

14. Claims 6, 8, 10 and 21 are allowed.

Response to Arguments

15. As per the applicants' argument that "Khang does not disclose a means for modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor", the Examiner takes the position that the applicants have not described the means for modeling the victim net in terms of the hardware

elements, software modules, the interface elements, the controllers, the memory elements, the display elements etc. If the applicants believe that the specification describes the means used by the apparatus, they are directed to indicate the page and paragraphs where the means are described and the figures which show the components of the means. The applicants only describe the method of modeling the victim net using two π-type resistor-capacitor (RC) circuits, including determining a coupling between the victim net and the aggressor.

The examiner has used a new reference **Rao** ("Delay analysis of the distributed RC line", IEEE, 1995). **Rao** teaches the method of modeling the victim net using two π-type resistor-capacitor (RC) circuits, including means for determining a coupling between the victim net and the aggressor (Page 5, CL1, Para 1, L7-14 and L30-35; Page 5, CL2, Para 2, L1-3 and L12-16; page 5, table 2; Page 6, Fig 2(c)), as higher order lumped approximations of distributed resistance and capacitance provide accurate predictions of 10% and 90% threshold crossing times; and the first order network underestimates the 10% crossing time by as much as 60%, while the second order network underestimates the 10% crossing time less than 22% (Page 1, CL1, Para 1, L12-15; Page 5, CL2, Para 2, L1-3 and L12-16).

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 14, 2005